IN THE CLAIMS:

Please AMEND claims 1-13, 15-25, 27-41 and 43-58 in accordance with the following:

1. (Currently Amended) An amplifier comprising amplification means ~~(AM)~~ comprising an input and an output,

said amplification means ~~(AM)~~ comprising a switching output stage delivering at least one output signal ~~(OUS)~~ via said output,

said amplification means being fed by power supply means ~~(PSM)~~,

said amplifier further comprising compensation means ~~(CM)~~ providing a compensation signal ~~(CS)~~ derived from the power supply voltage ~~(PSV)~~ of the power supply means ~~(PSM)~~,

said compensation signal ~~(CS)~~ comprising a substantially inverse representation of said power supply voltage ~~(PSV)~~ and

said compensation signal ~~(CS)~~ being fed to said amplification means ~~(AM)~~ via at least one multiplication point in which the compensation signal is multiplied with an input signal received from said input.

2. (Currently Amended) An amplifier according to claim 1, wherein said substantially inverse representation of the power supply voltage ~~(PSV)~~ is scaled by a ratio substantially corresponding to a desired amplification between the output and the input of the amplification means ~~(AM)~~.

3. (Currently Amended) An amplifier according to claim 1, wherein said compensation signal is established for maintaining a substantially fixed utility area of a period of the amplified pulse width modulated signal regardless of changes in the power supply voltage ~~(PSV)~~, wherein the fixed utility area means the area bounded by a graphical representation of a pulse of an output signal from said switching output stage, and wherein maintaining a substantially fixed utility area means that the utility areas that represent equal values of said input signal are maintained equal by means of the compensation signal regardless of changes in the power supply voltage.

4. (Currently Amended) An amplifier according to claim 1, wherein said ~~compensation means~~amplifier further comprises extrapolation means ~~(EM)~~ adapted for modifying said compensation signal ~~(CS)~~ according to a predefined extrapolation algorithm.

5. (Currently Amended) An amplifier according to claim 1, wherein said compensation signal ~~(CS)~~ is established on the basis of an inverting generator fed by a power supply comprising a circuit adapted for establishing an inverse signal of a voltage of said power supply, said inverting generator being comprised by said compensation means.

6. (Currently Amended) An amplifier according to claim ~~1~~5, wherein said inverting generator comprises at least one feedback loop having a power supply voltage dependent feedback.

7. (Currently Amended) An amplifier according to claim 5, wherein said inverting generator comprises

at least one forward path ~~(LF, MM, QM)~~ having an input and an output,

at least one reference oscillator ~~(SG)~~, and

at least one feedback path derived from said forward path and fed back to said input of said forward path by means of a summing point ~~(SP)~~ subtracting the feed-back signal from an input received from said reference oscillator ~~(SG)~~,

wherein said feedback path comprises a power supply voltage dependent feedback.

8. (Currently Amended) An amplifier according to ~~claim~~ 7, wherein said inverting generator outputs a digital signal on ~~the~~ an output ~~(PWCS)~~ of said forward path derived from at least one analog signal received in ~~said~~ an input ~~(PSVR)~~.

9. (Currently Amended) An amplifier according to claim 7, wherein said forward path comprises a limiter ~~(MM)~~ adapted for providing a pulse width modulated output signal ~~(PWCS)~~ of said forward path.

10. (Currently Amended) An amplifier according to claims ~~10~~9, wherein said forward path further comprises a time quantizer ~~(QM)~~ converting said pulse width modulated signal, preferably two-level, into a time discrete signal fed to the output ~~(PWCS)~~ of said forward path.

11. (Currently Amended) An amplifier according to claim 1, wherein said ~~compensation signal is fed to said amplification means via at least one multiplication point (MP) in which the compensation signal is multiplied with a preferably~~ input signal is a digital input signal ~~(IUS)~~.

12. (Currently Amended) An amplifier according to claim ~~11~~1, wherein said ~~compensation means~~amplifier further comprises decimation means ~~(DM)~~ adapted for transforming said compensation signal ~~(CS)~~ into compatibility with said input signal ~~(IUS)~~.

13. (Currently Amended) An amplifier according to claim 1, wherein ~~the~~ signal processing performed by said amplification means multiplicatively depends on the power supply voltage.

14. (Previously Presented) An amplifier according to claim 7, wherein said inverting generator comprises at least one self-oscillating loop.

15. (Currently Amended) An amplifier according to claim 14, wherein said self-oscillating loop comprises said at least one forward path ~~(LF, MM, QM)~~ and said at least one feedback path.

16. (Currently Amended) An amplifier according to claim 7, wherein said forward path comprises at least one loop filter ~~(LF)~~.

17. (Currently Amended) An amplifier according to claim 16, wherein said at least one loop filter ~~(LF)~~ is adapted to facilitate self-oscillation.

18. (Currently Amended) An amplifier according to claim 14, wherein a switch frequency of a pulse width modulated output signal ~~(PWCS)~~ provided by a limiter ~~(MM)~~ is at least partly defined by said at least one self-oscillating loop.

19. (Currently Amended) An amplifier according to claim 16, wherein an order of said at least one loop filter ~~(LF)~~ is at least ~~one~~first order.

20. (Currently Amended) An amplifier according to claim 16, wherein an order of said at least one loop filter ~~(LF)~~ is at least ~~two~~second order.

21. (Currently Amended) An amplifier according to claim ~~1~~5, wherein an effective order of an open loop transfer function of said inverting generator is at least one, preferably substantially two, wherein the effective order means a filter order apparent from the slope of a logarithmic frequency response gain plot of said open loop transfer function; said effective order preferably being derived by dividing a gradient of said plot by a gradient of a first-order transfer function.

22. (Currently Amended) An amplifier according to claim ~~18~~14, wherein a phase margin ~~(UPM)~~ of the open loop characteristic of said self-oscillating loop for frequencies within a frequency band starting from an upper limit of a utility frequency band and ending at the switch frequency is between 0° and 60°, more preferably between 0° and 45°, and even more preferably between 0° and 30°.

23. (Currently Amended) An amplifier according to claim 5, wherein said inverting generator ~~(CM)~~ comprises switch frequency control means.

24. (Currently Amended) An amplifier according to claim 23, wherein said switch frequency control means comprises an oscillating overlay signal generator connected to said at least one self-oscillating loop.

25. (Currently Amended) An amplifier according to claim ~~24~~7, wherein said reference oscillator ~~(SG)~~ provides a composite reference signal ~~(RS)~~ comprising a DC reference value and an oscillating overlay signal.

26. (Previously Presented) An amplifier according to claim 25, wherein said oscillating overlay signal comprises a peak-to-peak amplitude of less than 10% of said DC reference value, preferably less than 5% of said DC reference value.

27. (Currently Amended) An amplifier according to claim 10, wherein a clock frequency of said time quantizer ~~(QM)~~ is at least ten times greater than ~~said~~ a switch frequency of said pulse width modulated output signal provided by said limiter, preferably at least hundred times greater.

28. (Currently Amended) An amplifier according to claim 12, wherein said decimation means ~~(DM)~~ comprises an anti-aliasing filter having an impulse response which is longer than a period of ~~said~~ a pulse width modulated output signal established by a limiter and a time quantizer comprised by said compensation means ~~(PWCS)~~, preferably at least the length of two times the period of said pulse width modulated output signal ~~(PWCS)~~, and even more preferably at least the length of three times the period of said pulse width modulated output signal ~~(PWCS)~~.

29. (Currently Amended) An amplifier according to claim 28, wherein a stopband attenuation of said anti-aliasing filter of said decimation means ~~(DM)~~ is greater than 50dB, preferably greater than 70dB.

30. (Currently Amended) An amplifier according to claim 28, wherein said anti-aliasing filter of said decimation means ~~(DM)~~ comprises stopbands defined by:

$$\text{Stopband} = k \cdot f_{Sout} \pm BW,$$

where $k = 1, 2, 3, \ldots$ until the Nyquist frequency is reached, f_{Sout} is the output rate of the decimation means ~~(DM)~~ and BW is the utility bandwidth, e.g. 20 kHz.

31. (Currently Amended) An amplifier according to any of the claims 28, wherein said anti-aliasing filter of said decimation means ~~(DM)~~ comprises at least two, preferably three, cascaded running average FIR filters.

32. (Currently Amended) An amplifier according claim 31, wherein said anti-aliasing filter of said decimation means ~~(DM)~~ further comprises two half-band FIR filters.

33. (Currently Amended) An amplifier according to claim 6, wherein said power supply voltage dependent feedback comprises buffering means ~~(BM)~~.

34. (Currently Amended) An amplifier according to claim 33, wherein said buffering means ~~(BM)~~ comprises certain specifications substantially representing corresponding specifications of said amplification means ~~(AM)~~.

35. (Currently Amended) An amplifier according to claim 5, wherein said inverting generator is adapted for establishing at least one reciprocated electrical signal ~~(PWCS)~~, said inverting generator comprising at least one feedback loop, said at least one feedback loop comprising at least one forward path being fed by a reference signal ~~(RS)~~ and comprising at least one non-linearity ~~(MM)~~, and at least one feedback path comprising at least one variable amplifier ~~(BM)~~, wherein at least one of said at least one variable amplifier is controlled on the basis of an electrical signal ~~(PSVR)~~.

36. (Currently Amended) An amplifier according to claim 35, wherein at least one of said at least one feedback loop of said inverting generator comprises at least one quantization means ~~(QM)~~.

37. (Currently Amended) An amplifier according to claim 35, wherein at least one of said at least one feedback loop of said inverting generator comprises at least one digital-to-analog conversion means ~~(DAC)~~.

38. (Currently Amended) An amplifier according to claim 35, wherein at least one of said at least one feedback loop of said inverting generator comprises at least one loop filter ~~(LF)~~.

39. (Currently Amended) An amplifier according to claim 5, wherein at least one forward path of said inverting generator comprises at least one analog-to-digital converter ~~(QM)~~, preferably comprising at least one latch, and at least one of said at least one feedback path of said inverting generator comprises at least one digital-to-analog converter ~~(DAC)~~.

40. (Currently Amended) An amplifier according to claim 1, wherein said input receives at least one input signal ~~(IUS, IUS1, IUS2, … IUS6)~~.

41. (Currently Amended) An amplifier according to claim 1, wherein said input receives a composite signal, said composite signal comprises at least two input signals ~~(IUS1, ISU2, … IUS6)~~.

42. (Previously Presented) An amplifier according to claim 41, wherein said composite signal comprises two input signals, six signals, or eight signals.

43. (Currently Amended) An amplifier according to claim 40, wherein said amplification means ~~(AM)~~ comprises at least one channel amplification means ~~(AM1, AM2, … AM6)~~.

44. (Currently Amended) An amplifier according to claim 1, wherein said amplification means ~~(AM)~~ comprises two, five, six, seven or eight channel amplification means ~~(AM1, AM2, … AM6)~~.

45. (Currently Amended) An amplifier according to claim 1, wherein said amplification means ~~(AM)~~ delivers one output signal, two output signals, five output signals, six output signals, or eight output signals ~~(OUS, OUS1, OUS2, …. OUS6)~~ via said output.

46. (Currently Amended) An amplifier according to claim 43, wherein said compensation signal ~~(CS)~~ is fed to at least one of said at least one channel amplification means ~~(AM1, … AM6)~~ by multiplication with the corresponding said at least one input signal ~~(IUS, IUS1, … IUS6)~~.

47. (Currently Amended) An amplifier according to claim 4, wherein said extrapolation means ~~(EM)~~ comprises distributed extrapolation means ~~(EM1, … EM6)~~.

48. (Currently Amended) An amplifier according to ~~any of the~~ claim ~~46~~4, wherein said amplification means comprises at least one channel amplification means and said extrapolation means ~~(EM)~~ comprises distributed extrapolation means ~~(EM1, … EM6)~~, wherein said compensation signal is fed to at least one of said at least one channel amplification means ~~(AM1, … AM6)~~ by extrapolation by the corresponding said distributed extrapolation means ~~(EM1, … EM6)~~ and said multiplication with the corresponding said at least one input signal ~~(IUS, IUS1, … IUS6)~~.

49. (Currently Amended) Method for compensating errors of a power signal ~~(PS)~~ comprising a power supply voltage ~~(PSV)~~, comprising

performing multiplicatively power supply voltage dependent signal processing on an input utility signal ~~(IUS)~~ by means of amplification means ~~(AM)~~,

establishing a compensation signal ~~(CS)~~ comprising a representation of the ratio between a desired voltage ~~(DV)~~ and said power supply voltage ~~(PSV)~~, and

applying said compensation signal ~~(CS)~~ to said input utility signal ~~(IUS)~~ by means of multiplication.

50. (Currently Amended) Method for compensating errors of a power signal according to claim 49, whereby said establishment of a compensation signal ~~(CS)~~ comprises

establishing a forward path fed by a reference signal ~~(RS)~~,

establishing a negative feedback path from the output ~~(PWCS)~~ of said forward path, and

scaling the signal of said feedback path proportionally with a representation ~~(PSVR)~~ of said power supply voltage ~~(PSV)~~.

51. (Currently Amended) Method for compensating errors of a power signal according to claim 49, whereby said establishment of ~~a~~ the compensation signal ~~(CS)~~ comprises

providing an electrical signal ~~(PSVR)~~,

providing at least one feedback loop comprising

at least one forward path comprising at least one non-linearity ~~(MM)~~ and

at least one feedback path comprising at least one variable amplifier ~~(BM)~~, and

feeding to at least one of said at least one variable amplifier said electrical signal ~~(PSVR)~~.

52. (Currently Amended) Method for compensating errors of a power signal according to claim ~~50~~51, whereby at least one of said at least one forward path is fed with at least one reference signal ~~(RS)~~.

53. (Currently Amended) Method for compensating errors of a power signal according to claim 51, whereby at least one of said at least one feedback loop comprises at least one quantization means ~~(QM)~~.

54. (Currently Amended) Method for compensating errors of a power signal according to claim 51, whereby at least one of said at least one feedback loop comprises at least one digital-to-analog conversion means ~~(DAC)~~.

55. (Currently Amended) Method for compensating errors of a power signal according to claim 53, whereby quantization noise introduced by at least one of said at least one quantization means ~~(QM)~~ is shaped by at least one loop filter ~~(LF)~~.

56. (Currently Amended) Method for compensating errors of a power signal according to claim 52, whereby said reference signal ~~(RS)~~ is an oscillating voltage signal.

57. (Currently Amended) Method for compensating errors of a power signal according to claim 51, whereby said non-linearity ~~(MM)~~ is a limiter.

58. (Currently Amended) Method for compensating errors of a power signal according to claim 51, whereby said non-linearity ~~(MM)~~ is a comparator.